UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/930,365 | 08/15/2001 | Masahiro Takeuchi | 15.45/6059 | 3437 |

24033 7590 03/14/2003

KONRAD RAYNES VICTOR & MANN, LLP
315 SOUTH BEVERLY DRIVE
SUITE 210
BEVERLY HILLS, CA 90212

| EXAMINER | |
|---|---|
| VU, QUANG D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/930,365 | TAKEUCHI, MASAHIRO | |
| | Examiner | Art Unit | |
| | Quang D Vu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amendment filed on 12/27/02* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7-26 and 32-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-23,26 and 32-37* is/are rejected.

7)☒ Claim(s) *24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-5, 14-15, 18 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,165,854 to Wu.

Regarding claim 1, Wu (figures 1-9) teaches a method for manufacturing a semiconductor device having a trench isolation region (10, 12, 14), the method comprising the steps of:

forming a trench (8) in a semiconductor layer (2);

forming a dielectric layer (14) that fills the trench (8);

conducting a thermal treatment of the dielectric layer (14), wherein the thermal treatment is conducted at a temperature of 1100° C; and

forming a well (the source or drain region of the CMOS transistor) in the semiconductor layer (2), and conducting the thermal treatment of the dielectric layer (14) before forming the well in the semiconductor layer (2).

Regarding claim 3, Wu teaches the temperature of the thermal treatment is 1100° C (column 4, lines 26-38).

Regarding claim 4, Wu teaches the temperature of the thermal treatment is in the range of 1050° C to 1100° C.

Regarding claim 5, Wu teaches the dielectric layer (14) is formed by a high density plasma chemical vapor deposition method (column 4, lines 26-30).

Regarding claim 14, Wu (figures 1-9) teaches a method for manufacturing a semiconductor device having a trench isolation region (10, 12, 14), the method comprising:

forming a trench (8) in a semiconductor layer (2);

forming a dielectric layer (14) in the trench (8); and

heating the dielectric layer (14) at a temperature of 1100°; and

forming a well (the source or drain region of the CMOS transistor) in the semiconductor layer (2) adjacent to the trench (8) after the heating the dielectric layer (14) at a temperature of 1100°C.

Regarding claim 15, Wu teaches a method further comprising: forming a trench oxide layer (10) on the sidewalls and bottom of the trench (8) prior to forming the dielectric layer (14) in the trench.

Regarding claim 18, Wu teaches a method further comprising: forming at least one transistor (a CMOS transistor) adjacent to the trench isolation region, the at least one transistor being formed after heating the dielectric layer (14) at a temperature of 1100 ° C.

Regarding claim 32, Wu (figures 1-9) teaches a method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer (2);

forming a plurality of trenches (8) in the semiconductor layer (2);

forming a thermal oxide layer (10) on the semiconductor surface in the trenches (8);

depositing a dielectric layer (14) into the trenches (8) and filling the trenches (8) with the dielectric layer (14);

thermally treating the dielectric layer (14) in the trenches at a temperature of 1100 °C; and

after the thermally treating the dielectric layer (14) in the trenches (8), forming a well (the source or drain region of the CMOS transistor) region between adjacent trenches.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2,13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,165,854 to Wu.

Regarding claim 2, Wu differs from the claimed invention by not showing the dielectric layer is formed with a film density of at least 2.1 g/cm$^3$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at lest 2.1 g/cm$^3$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, Wu differs from the claimed invention by not showing the trench is formed with a trench width of no greater than 0.35 micrometer. It would have been obvious to

one having ordinary skill in the art at the time the invention was made for the trench is formed with a trench width of no greater than 0.35 micrometer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 16, Wu teaches the trench oxide layer (10) is formed by oxidizing the sidewalls and bottom surface of the trench. Wu differs from the claimed invention by not showing the trench oxide layer is formed to have a thickness in the range of 10 nm to 100 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the trench oxide layer is formed to have a thickness in the range of 10 nm to 100 nm, since it ahs been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 17, Wu differs from the claimed invention by not showing the heating of the dielectric layer is carried out for a time in the range of 20 minutes to 120 minutes at a temperature in the range of 1050°C to 1200°C. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the heating of the dielectric layer is carried out for a time in the range of 20 minutes to 120 minutes at a temperature in the range of 1050°C to 1200°C because it depends on the desired dielectric constant of the dielectric layer.

5. Claims 1 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al.

Regarding claim 1, Chen et al. (figures 2A – 2G) teach a method for manufacturing a semiconductor device having a trench isolation region (224), the method comprising the steps of:

forming a trench (218) in a semiconductor layer (200);

forming a dielectric layer (222) that fills the trench (218);

conducting a thermal treatment of the dielectric layer (222), wherein the thermal treatment is conducted at a temperature of 1000° C;

forming a well (228) in the semiconductor layer, and the thermal treatment is conducted before forming the well in the semiconductor layer.

Chen et al. teach conducting a thermal treatment of the dielectric layer (222) at a temperature of 1000° C. Chen et al. differ from the claimed invention by not showing the thermal treatment of the dielectric layer is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment of the dielectric layer is conducted at a temperature of at least 1050° C because it depends on the desired dielectric constant of the dielectric layer.

Regarding claim 7, Chen et al. teach the trench (216, 218) includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer (220) thereon (column 5, lines 7-10), wherein the dielectric layer (222) is formed in direct contact with the thermal oxide layer (220).

Regarding claim 8, Chen et al. teach thermally oxidizing the sidewall surfaces and the bottom surface of the trench (column 5, lines 7-10). Chen et al. differ from the claimed invention by not showing thermally oxidizing the sidewall surfaces and the bottom surface of the

trench is carried out at a temperature in the range of at 700° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally oxidizing the sidewall surfaces and the bottom surface of the trench at a temperature in the range of at 700° C to 1150° C because it depends of the desired dielectric constant of the dielectric layer.

Regarding claim 9, Chen et al. teach thermally oxidizing the sidewall surfaces and the bottom surface of the trench (column 5, lines 7-10). Chen et al. differ from the claimed invention by not showing thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 950° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally oxidizing the sidewall surfaces and the bottom surface of the trench at a temperature in the range of at 950° C to 1150° C because it depends of the desired dielectric constant of the dielectric layer.

Regarding claim 10, Chen et al. teach thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer (220) having a thickness in the range of 20nm to 90nm (column 5, lines 7-10).

6. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,165,854 to Wu as applied to claim 1 above, and further in view of US Patent No. 6,087,243 to Wang.

Regarding claim 11, Wu differs from the claimed invention by not showing the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate.

However, Wang (figures 1A – 1H) teaches the semiconductor substrate comprises an epitaxial growth layer (11) formed on a semiconductor substrate (10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an epitaxial layer of Wang into the substrate taught by Wu because it depends on the electrical characteristic of device.

Regarding claim 12, Wu and Wang differ form the claimed invention by not showing the epitaxial growth layer has a thickness of at least 2 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the epitaxial growth layer has a thickness of at least 2 micrometer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al.

Regarding claim 19, Chen et al. (figures 2A-2G) teach a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a first layer (210) on a semiconductor substrate (200);

forming a polishing stopper layer (214) above the first layer (210);

forming at least one trench (218) by etching the first layer (210) while using the polishing stopper layer (214) as a mask;

forming a dielectric layer (222) in and above the trench; and

planarizing the dielectric layer (222) using the polishing stopper layer (214) as a stopper;

heating the dielectric layer (222) to a temperature of 1000° C;

after heating the dielectric layer (222) to a temperature about 1000° C, forming a well (228) in the semiconductor substrate (200) adjacent to the trench (218).

Chen et al. teach heating the dielectric layer (222) to a temperature about 1000° C. Chen et al. differ from the claimed invention by not showing heating the dielectric layer to a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for heating the dielectric layer to a temperature of at least 1050° C because it depends on the desired dielectric constant of the dielectric layer.

Regarding claim 21, Chen et al. teach removing a portion of the polishing stopper layer (214) after planarizing the dielectric layer (222).

8. Claims 19, 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al. in view of US Patent No. 6,087,243 to Wang.

Regarding claims 19 and 20, Chen et al. (figures 2A-2G) teach a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a polishing stopper layer (214) above the substrate (200);

forming at least one trench (218) by etching the first layer (210) while using the polishing stopper layer (214) as a mask;

forming a dielectric layer (222) in and above the trench; and

planarizing the dielectric layer (222) using the polishing stopper layer (214) as a stopper;

heating the dielectric layer (222) to a temperature of 1000° C;

after heating the dielectric layer (222) to a temperature about 1000° C, forming a well (228) in the semiconductor substrate (200) adjacent to the trench (218).

Chen et al. teach heating the dielectric layer (222) to a temperature about 1000° C. Chen et al. differ from the claimed invention by not showing heating the dielectric layer to a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for heating the dielectric layer to a temperature of at least 1050° C because it depends on the desired dielectric constant of the dielectric layer.

Chen et al. differ from the claimed invention by not showing the first layer comprises an epitaxial growth layer. However, Wang (figures 1A – 1H) teaches the semiconductor substrate comprises an epitaxial growth layer (11) formed on a semiconductor substrate (10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an epitaxial layer of Wang into the substrate taught by Wu because it depends on the electrical characteristic of device.

Regarding claim 22, the combined method teaches oxidizing at least a portion of the first layer in the at least one trench prior to forming the dielectric layer in and above the trench.

Regarding claim 23, the combined method teaches forming a pad layer between the first layer and the polishing stopper layer.

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al. as applied to claim 19 above, and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 26, Chen et al. differ from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the high density plasma chemical vapor deposited dielectric layer of Wu into the method taught by Chen et al. because it improves the dielectric property of the dielectric layer.

10. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al.

Regarding claim 32, Chen et al. teach a method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer (200);

forming a plurality of trenches (216, 218) in the semiconductor layer (200);

forming a thermal oxide layer (220) on the semiconductor surface in the trenches (216, 218);

depositing a dielectric layer (222) into the trenches (216, 218) and filling the trenches (216, 218) with the dielectric layer (222);

thermally treating the dielectric layer (14) in the trenches at a temperature about 1000 $^{o}$C; and

after the thermally treating the dielectric layer (222) in the trenches (216, 218), forming a well (228) region between adjacent trenches (216, 218).

Chen et al. differ from the claimed invention by not showing thermally treating the dielectric layer in the trenches at a temperature of at least 1050 ° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally treating the dielectric layer at a temperature of at least 1050 ° C because it depends on the desired dielectric constant of the dielectric layer.

Regarding claim 33, Chen et al. teach the dielectric layer (222) is formed in direct contact with the thermal oxide layer (220) in the trenches (216, 218).

Regarding claim 34, Chen et al. differ from the claimed invention by not showing the dielectric layer is formed with a film density of at lest 2.1 $g/cm^3$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at lest 2.1 $g/cm^3$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

11. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,950,090 to Chen et al. as applied to claim 34 above, and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 35, Chen et al. differ from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the high density plasma chemical vapor

deposited dielectric layer of Wu into the method taught by Chen et al. because it improves the dielectric property of the dielectric layer.

12. Claims 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. and Wu as applied to claim 35 above, and further in view of US Patent No. 6,087,243 to Wang.

Regarding claim 36, Chen et al. and Wu differ from the claimed invention by not showing the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate. However, Wang (figures 1A – 1H) teaches the semiconductor substrate comprises an epitaxial growth layer (11) formed on a semiconductor substrate (10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an epitaxial layer of Wang into the substrate taught by Chen et al. and Wu because it depends on the electrical characteristic of device.

Regarding claim 37, Chen et al., Wu and Wang differ form the claimed invention by not showing a method, wherein the epitaxial growth layer has a thickness of at least 2 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the epitaxial growth layer has a thickness of at least 2 micrometer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

***Allowable Subject Matter***

Claims 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-5, 7-23 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
March 10, 2003

Steven Loke